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Attorney Docket No. 18865-35US
Client Ref No. 17732-9833

ASSISTANT COMMISSIONER FOR PATENTS
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Sir:

Transmitted herewith for filing is the
[**X**] patent application of

Inventor(s)/Applicant Identifier: Maria Clemens Y. Quinones et al.

For: IMPROVED METHOD OF MAKING A CHIP DEVICE

Enclosed are:
[**X**] 11 sheet(s) of [ ] formal [**X**] informal drawing(s).
[**X**] A [ ] signed [**X**] unsigned Declaration.

In view of the Unsigned Declaration as filed with this application and pursuant to 37 CFR §1.53(d), Applicant requests deferral of the filing fee until submission of the Missing Parts of Application.

DO NOT CHARGE THE FILING FEE AT THIS TIME.

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Attorney Docket No.: 18865-35US
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PATENT APPLICATION

IMPROVED METHOD OF MAKING A CHIP DEVICE

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IMPROVED METHOD OF MAKING A CHIP DEVICE

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates to an improved method of making a chip device, and more particularly, an improved method of packaging a plurality of DMOS devices and an arrangement for making a plurality of DMOS devices.

2. Description Of The Prior Art

Semiconductor power switching devices, and particularly, power MOSFET devices continue to push the lower limits of on-state resistance. While silicon process technology has advanced significantly in the past decade, essentially the same decades old package technology continues as the primary packaging means. Epoxy or soldered die attach along with aluminum or gold wire interconnects is still a preferred power device package methodology.

Recently, chip devices have been manufactured and packaged by connecting the chip within the device to the leads directly through a low resistance solder connection. By using a second leadframe element and solder to connect the device conductors and the first leadframe, a direct connection is enabled. Furthermore, the size and shape of the second leadframe may be tailored to fit the chip device and to minimize its electrical and thermal resistance.

Thus, it is desirable to provide a method and arrangement for making such "wireless" packaging of chip devices manufacturable in a high volume production environment.

SUMMARY OF THE INVENTION

In accordance with one aspect of the present invention, a method of making a plurality of DMOS devices includes providing a plurality of bottom leadframes coupled to one another with a pair of rails, attaching a corresponding bumped die

including a plurality of solder bumps thereon including a source and gate array to each bottom leadframe, and placing a plurality of top leadframes on the bumped dies such that each top leadframe contacts solder bumps on a corresponding bumped die, the plurality of top leadframes being coupled to one another with a pair of rails.

In accordance with another aspect of the present invention, the method further includes placing a molded body around each top and bottom leadframe with a corresponding bumped die therebetween.

In accordance with another aspect of the present invention, the method includes spot welding a rail at the bottom leadframe and a rail of the top leadframe together.

In accordance with a further aspect of the present invention, the method includes pressfitting a rail on the bottom leadframe and a rail on the top leadframe together.

In accordance with yet another aspect of the present invention, the bumped die is attached to the bottom leadframe with an adhesive wherein the adhesive is cured sometime during the method after the bumped die is attached thereto.

In accordance with a further aspect of the present invention, a plurality of DMOS devices includes a plurality of bottom leadframes that each contain a plurality of leads, a plurality of bumped dies, each bumped die being on a corresponding bottom leadframe and including a source and gate array, and a plurality of top leadframes, each top leadframe being coupled to a corresponding bumped die and including a plurality of leads. The plurality of DMOS devices further includes four rails, a first rail being connected to a first side of each of the top leadframes, a second rail being connected to a second side of each of the top leadframes, a third rail being connected to a first side of each of the bottom leadframes, and a fourth rail being connected to a second side of each of the bottom leadframes. The bottom leadframe has leads coupled to drain terminals on the bumped die, the top leadframe has a lead coupled to a gate terminal on the bumped die, and leads coupled to source terminals on the bumped die, and the first rail is coupled to the third rail while the second rail is coupled to the fourth rail.

Thus, the present invention provides a method for packaging "wireless" chip devices in a high volume production environment. The method provides improved heat dissipation, excellent lead co-planarity control, low lead stress trim and form process, no loose metals at the trim and form process, unidirectional mold gating for

better cavity fill and less compound flow turbulence, better manufacturability , and a flexible bumped die attach process.

Other features and advantages of the present invention will be understood upon reading and understanding the detailed description of the preferred exemplary embodiments, found hereinbelow in conjunction with reference to the drawings in which like numerals represent like elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a perspective view of a chip device made in accordance with the present invention;

Figure 1A is a schematic side sectional view of a bumped die;

Figure 2A is a perspective view of a bottom leadframe for use in making a chip device in accordance with the present invention;

Figure 2B is a perspective view of a bottom leadframe with die attach material thereon;

Figure 3A is a perspective view of a bottom leadframe with a die placed thereon;

Figure 3B is a perspective view of the bottom leadframe and die of Figure 3A with solder bumps added thereon;

Figure 4A is a perspective view of an inverted top leadframe for use in making a chip device in accordance with the present invention;

Figure 4B is a perspective view of the top leadframe placed on the bottom leadframe with the die and solder bumps therebetween;

Figure 5A is a schematic illustration of a bottom leadframe assembly for use in making chip devices in accordance with the present invention;

Figure 5B is a perspective view of a bottom leadframe of the bottom leadframe assembly illustrated in Figure 5A;

Figure 6A is a schematic illustration of a top leadframe assembly for use in making chip devices in accordance with the present invention;

Figure 6B is a perspective view of a top leadframe of the top leadframe assembly illustrated in Figure 6A;

Figure 7 is a perspective view of a bottom leadframe of the bottom leadframe assembly illustrated in Figure 5B, including bottom frame aligners; and

Figure 8 is a top leadframe from the top leadframe assembly illustrated in Figure 6B, including top frame aligners.

DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

In accordance with the present invention, a chip device 10 includes a bottom leadframe 11, a die 12, a top leadframe 13 and a molded body 14 that surrounds most of the leadframes with the die therebetween.

The bottom leadframe generally includes a die attach pad 15. The die attach pad is generally supported by tie bars 20 and a plurality of leads 21 that generally serve as the drain terminals. In a preferred embodiment, there are four leads. The bottom leadframe is preferably made of a copper alloy and the die attach pad is preferably plated with one of either Ag or Ni.

The die is preferably attached to the die attach pad with Ag-filled adhesives or soft solder 27. Examples of Ag-filled adhesives include epoxy and polyimide. The die includes a source and gate array along its top surface.

Generally, solder bumps 22 are placed on the top surface of the die. Preferably, the top surface of the die includes locations 23 defined therein for receiving the solder bumps. Preferably, the solder bumps are one of alloys that include Pb/Sn, Pb/Sn/Ag, Sn/Sb or an equivalent. Generally, each solder bump has a diameter of approximately .008 inches and a height of .006 inches.

Die 12 is preferably a one-piece item that is often referred to in the art as a "bumped die." As can be seen in Figure 1A, a bumped die includes die 12, "under bump material" that serves as an intermediate layer 26 between the top surface of the die and solder bump 22, and the solder bumps themselves. Preferably, the under bump material is one of TiW, Cu, Au or an equivalent. In the example illustrated in Figure 1A, the under bump material is broken into three layers—Cu plating 26a, sputtered Cu 26b and sputtered Ti 26d.

The top leadframe includes a plurality of pad protrusions 24 that are coupled to corresponding leads 25. Some of the pads are source pads 24s for engaging the source array on the die while one of the pads is a gate pad 24g for coupling to the gate area on the die.

The molded body generally consists of two pieces 30, 31, each having a length of approximately .193 inches, a width of .154 inches and, a combined height of .057 inches.

In accordance with present invention, a plurality of bottom leadframes 11 are coupled together with a pair of rails 40, 41 to form a bottom leadframe assembly as illustrated in Figure 5A. Figure 5B illustrates a typical bottom leadframe and how it is coupled between the two rails. The rails provide mechanical support for the bottom leadframe during the manufacturing process.

As noted previously, each bottom leadframe includes a die attach pad that provides connection to the drain of the die. Drain leads 21 are provided for connection of the drain to the die. A tie bar is provided for die attach pad support and package support at the early stages of forming the chip devices. A dambar 44 is also provided and serves as a mold flash barrier. A rail "up" set is provided as seen at 43 and levels drain leads 21 with gate and source leads 25 of a corresponding top leadframe. Preferably, at least one rail is provided with an index/alignment hole 42 for aligning the top and bottom leadframes and for use in transporting the rails during the manufacturing process. As can be seen in the figures, the index/alignment holes of rail 40 are preferably offset with respect to the index/alignment holes of rail 41.

With regard to Figure 6A, a plurality of top leadframes 13 coupled to one another between two rails 50, 51 to form a top lead frame assembly is illustrated. Figure 6B illustrates a typical top leadframe coupled between the two rails. The rails provide mechanical support of the top leadframe during the manufacturing process.

As noted previously, each top leadframe includes a source pad that includes terminals for connecting to source metalizations on the die and a gate pad for connecting one terminal to the gate metalization of the die. The pads each include contact protrusions for providing good contact between solder bumps of the die and the source/gate pads. The pads are in communication with corresponding leads 25. Once again, a dambar 54 is provided that serves as a mold flash barrier and support for the leads coplanarity. Each top leadframe also includes a lead "up" set as seen at 53 that provides space for the solder bumped die and for leveling the gate and source leads 25 with the drain leads 21 of the bottom leadframe. Index/alignment holes 52 are preferably provided in the rails to help ensure proper alignment between the rails of the top lead frame assembly and the rails of the bottom leadframe assembly. So that the alignment is

proper, the index/alignment holes of rail 51 are offset with respect to the index/alignment holes of rail 50. As should be readily apparent, the index/alignment holes of rail 40 align with the index/alignment holes of rail 51 while the index/alignment holes of rail 41 align with the index/alignment holes of rail 50 during the manufacturing process.

The rails of the two leadframes may include an easy-align feature to aid in aligning the index/alignment holes. The bottom frame aligners 60 are located on the bottom leadframe rails as illustrated in Figure 7. They may be of any suitable shape and size. Preferably, the bottom frame aligners protrude on the rail surface by approximately 50% to 75% of the leadframe thickness. Corresponding holes 61 are defined within the rails of the top leadframe assemblies and serve as top frame aligners as illustrated in Figure 8. These holes are of the same shape and size as the bottom frame aligners and are located on the same center lines as the bottom frame aligners. The bottom frame aligners are then pressfitted into the top frame alignment holes keeping both leadframe assemblies coupled to one another.

Alternatively, the rails of the leadframe assemblies may be spot welded near the location of the aligners. In such an embodiment, the aligners would not be of any particular shape but rather, would mark where the rails are to be spot welded to one another, or may be eliminated altogether.

In accordance with one embodiment of the present invention, a plurality of chip devices is manufactured by providing a bottom leadframe assembly. A bumped die 12 is placed on each die attach pad of each bottom leadframe and is attached thereto with epoxy. Generally, the bumped die will be required to be placed with approximately $\pm$ 2 mils accuracy. The epoxy is cured, such as, for example, by conventional box oven curing or heater block snap curing. As can be seen in Figure 3B, the solder bumps are in a row with one of the solder bumps slightly offset. This offset solder bump 22g corresponds to the gate area of the die. The top leadframe assembly receives flux (or is "fluxed") on its pads and is then flipped onto the bottom leadframe assembly such that a source pad and gate pad of each top leadframe engages a corresponding solder bump die gate and source array. Preferably, the rails of the top leadframe and the rails of the bottom leadframe are spot welded together. Other forms of coupling the rails of the top leadframe to the rails of the bottom leadframe may be used, including, for example, pressfitting.

The coupled top and bottom leadframe assemblies are then heated to reflow the solder bumps and permanently attach each die to its corresponding top leadframe.

In an alternative embodiment, the bumped die is attached to the die attach pad with an epoxy.

In another alternative embodiment, the top leadframe assembly is fluxed. Bumped dies 12 are then flipped from their pickup positions and attached to the top leadframes so that the source and gate arrays engage the source and gate pads. Once again, the die placement precision requirement is preferably $\pm$ 2 mils. The flipped dies and top leadframe assemblies are heated to reflow the solder bumps and permanently attach the dies to the top leadframes. Low melting solder paste or epoxy is dispensed on each die attach pad of the bottom leadframes and the top leadframe assembly is then flipped over onto the bottom leadframe assembly so that each die is attached to a corresponding die attach pad of a bottom leadframe. Preferably, the entire assembly is done on a heated block. Alternatively, the completed assembly may be cured in a conventional box oven. The top and bottom leadframe rails are preferably spot welded together.

Alternatively, any of the above methods may be performed with the fluxing being performed directly on the solder bumps of the bumped dies instead of the top leadframes. Additionally, the bottom leadframe assembly may be flipped onto the top leadframe assembly.

Each of the above methods are preferably preformed on a pick and place machine, or a similar type machine, as is known in the industry. Generally, the top and bottom leadframe assemblies will be positioned and held in place by the alignment/index holes.

Additionally, each of the above methods include placing a molded body around the "sandwiched leadframe assemblies." The dambars and mold flashes are mechanically removed and any remaining resin bleeds on the leads are removed using pressurized media to deflash grits. If desired, laser marking or marking with ink is preformed on a top surface of the molded bodies in order to identify the parts. Rack plating is then performed and the individual chip devices are removed from the frames and rails with the leads being trimmed and formed. Preferably, the trim and form is preformed with a three stage forming process as is known in the art.

Each of the top leadframes preferably includes slots defined in the source and gate pads to facilitate a good contact and alignment with the solder bumps between the die and the top leadframe. These slots also provide a sufficient mold plastic path. Alternatively, the top leadframes may include punch-through holes as opposed to slots.

Accordingly, the present invention provides methods by which "wireless" packaging is made manufacturable in a high volume production environment. The methods allow for improved heat dissipation, excellent lead coplanarity control, low lead stress trim and form process, reduced loose metals during the trim and form process and overall better manufacturability.

Although the invention has been described with reference to specific exemplary embodiments, it will appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A plurality of chip devices comprising:

a plurality of bottom leadframes each including a plurality of leads;

a plurality of bumped dies, each bumped die being on a corresponding bottom leadframe and including a source and gate solder bump array;

a plurality of top leadframes, each top leadframe being coupled to a corresponding bumped die and including a plurality of leads; and

four rails, a first rail being connected to a first side of each of the top leadframes, a second rail being connected to a second side of each of the top leadframes, a third rail being connected to a first side of each of the bottom leadframes, and a fourth rail being connected to a second side of each of the bottom leadframes;

wherein each bottom leadframe has leads coupled to drain terminals on its corresponding bumped die;

wherein each top leadframe has a lead coupled to a gate terminal on its corresponding bumped die and leads coupled to source terminals on its corresponding die; and

wherein the first rail is coupled to the third rail and the second rail is coupled to the fourth rail.

2. An arrangement in accordance with claim 1 wherein the solder bumps consist of one of Pb-Sn, Pb-Sn-Ag or Sn-Sb.

3. An arrangement in accordance with claim 1 wherein the leads are coupled to the gate terminal and the source terminals via pads.

4. An arrangement in accordance with claim 1 further comprising a plurality of molded bodies, each body encapsulating a portion of a corresponding top leadframe and a corresponding bottom leadframe, and a corresponding bumped die therebetween.

5. An arrangement in accordance with claim 1 wherein the chip devices are DMOS devices.

6. An arrangement in accordance with claim 1 wherein the top leadframes include slots defined therein.

7. A method of making a chip device, the method comprising:

providing a plurality of bottom leadframes coupled to one another with a pair of rails;

attaching a corresponding bumped die including a source and gate solder bump array to each bottom leadframe;

providing a plurality of top leadframes coupled to one another with a pair of rails; and

flipping the plurality of top leadframes such that each top leadframe contacts the solder bumps on a corresponding bumped die,.

8. A method in accordance with claim 7 further comprising placing a molded body around each top and bottom leadframe with a corresponding bumped die therebetween.

9. A method in accordance with claim 7 further comprising spot welding a rail of the bottom leadframe and a rail of the top leadframe together.

10. A method in accordance with claim 9 further comprising reflowing the solder bumps.

11. A method in accordance with claim 7 further comprising pressfitting a rail of the bottom leadframe and a rail of the top leadframe together.

12. A method in accordance with claim 11 further comprising reflowing the solder bumps.

13. A method in accordance with claim 7 wherein the bumped die is attached to the bottom leadframe with an adhesive, the adhesive being cured sometime during the method after the die is attached thereto.

14. A method in accordance with claim 7 wherein the bumped die is attached to the bottom leadframe with soft solder.

15. A method of making a plurality of chip devices, the method comprising:

providing a plurality of top leadframes coupled to one another with a pair of rails;

flipping a bumped die including a source and gate solder bump array on each top leadframe such that each bumped die contacts the gate and source pads of topframe; and

providing a plurality of bottom leadframes being coupled to one another with a pair of rails;

flipping the top leadframes onto the plurality of bottom leadframes such that a bumped die is between each top leadframe and a corresponding bottom leadframe.

16. A method in accordance with claim 15 further comprising placing a molded body around each top and bottom leadframe with a corresponding bumped die therebetween.

17. A method in accordance with claim 15 further comprising spot welding a rail of the bottom leadframe and a rail of the top leadframe together.

18. A method in accordance with claim 17 further comprising reflowing the solder bumps.

19. A method in accordance with claim 15 further comprising pressfitting a rail of the bottom leadframe and a rail of the top leadframe together.

20. A method in accordance with claim 19 further comprising reflowing the solder bumps.

21. A method in accordance with claim 15 wherein the die is attached to the bottom leadframe with soft solder.

22. A method in accordance with claim 15 wherein the die is attached to the bottom leadframe with an adhesive, the adhesive being cured sometime during the method after the die is attached thereto.

23. A method of making a plurality of chip devices, the method comprising:

providing a plurality of top leadframes coupled to one another with a pair of rails;

providing a plurality of bottom leadframes coupled to one another with a pair of rails, each bottom leadframe including a die attach pad;

placing a bumped die including a source and gate array on each die attach pad of each bottom leadframe; and

coupling the top and bottom leadframe rails together such that each bumped die contacts the solder bumps of a corresponding top leadframe.

24. A method in accordance with claim 23 further comprising placing a molded body around each top and bottom leadframe with a corresponding bumped die therebetween.

25. A method in accordance with claim 23 further comprising spot welding the rails of the bottom leadframe and the rails of the top leadframe together.

26. A method in accordance with claim 25 further comprising reflowing the solder bumps.

27. A method in accordance with claim 23 further comprising pressfitting the rails of the bottom leadframe and the rails of the top leadframe together.

28. A method in accordance with claim 27 further comprising reflowing the solder bumps.

29. A method in accordance with claim 23 wherein each bumped die is attached to the bottom leadframe with an adhesive, the adhesive being cured sometime during the method after the die is attached thereto.

30. A method in accordance with claim 23 wherein each bumped die is attached to the bottom leadframe with soft solder.

IMPROVED METHOD OF MAKING A CHIP DEVICE

ABSTRACT OF THE DISCLOSURE

A method and arrangement for packaging a plurality of chip devices. The method includes providing a plurality of bottom leadframes coupled together with rails to form a bottom leadframe assembly and providing a plurality of top leadframes coupled together with rails to form a top leadframe assembly. Dies are placed between the top and bottom leadframes and the top and bottom leadframe assemblies are coupled to one another. The dies are attached to die attach pads of the bottom leadframes and are coupled to the top leadframes with solder bumps. A molded body is placed around the top and bottom leadframes with the dies therebetween and the rails are removed from the top and bottom leadframes, thus providing a plurality of chip devices.

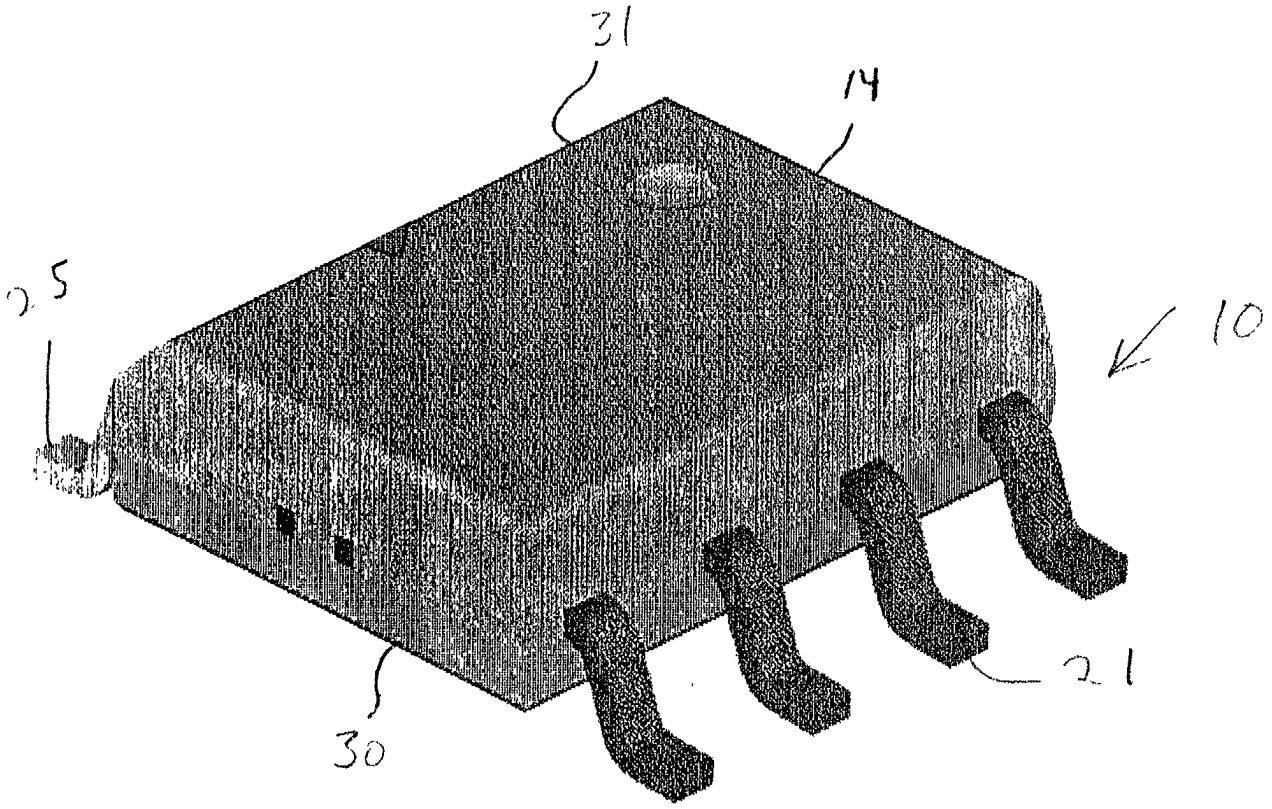

Figure 1

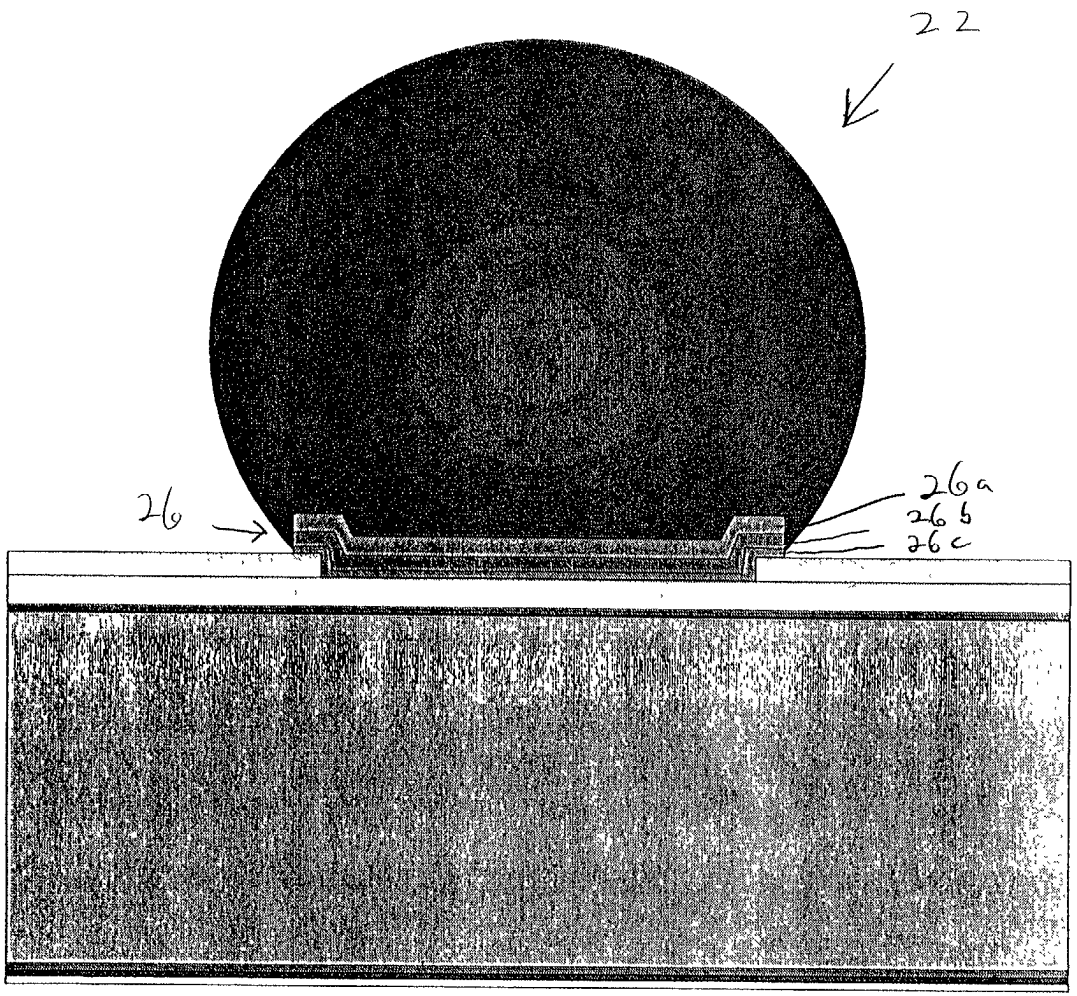

Figure 1A

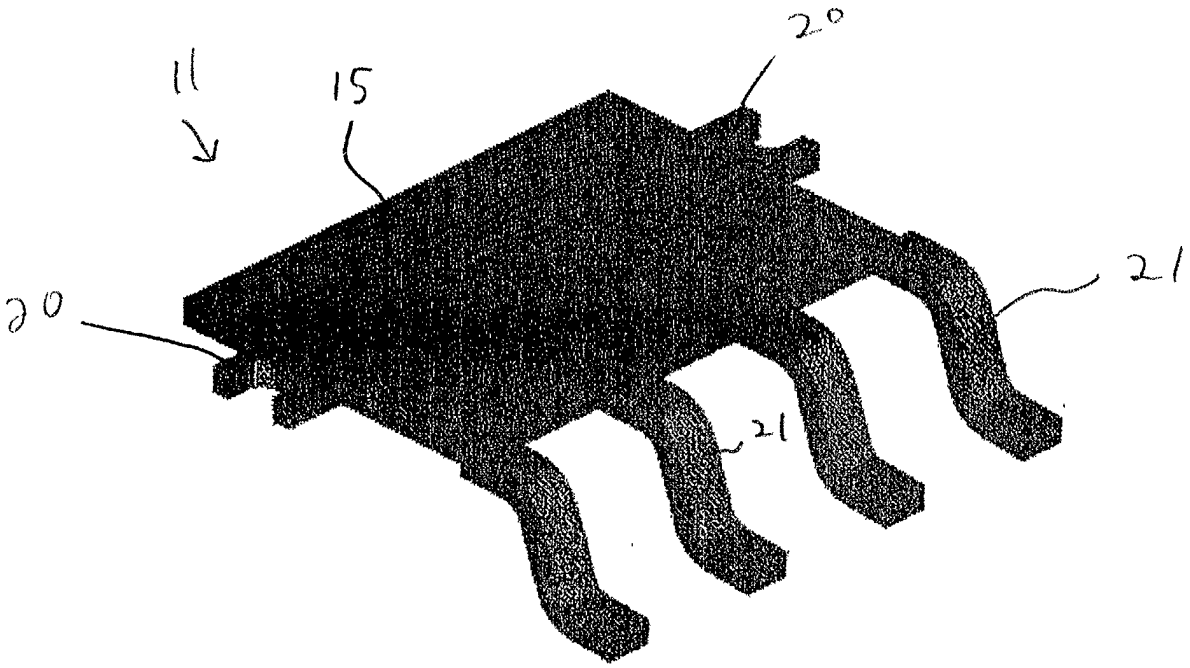

Figure 2A

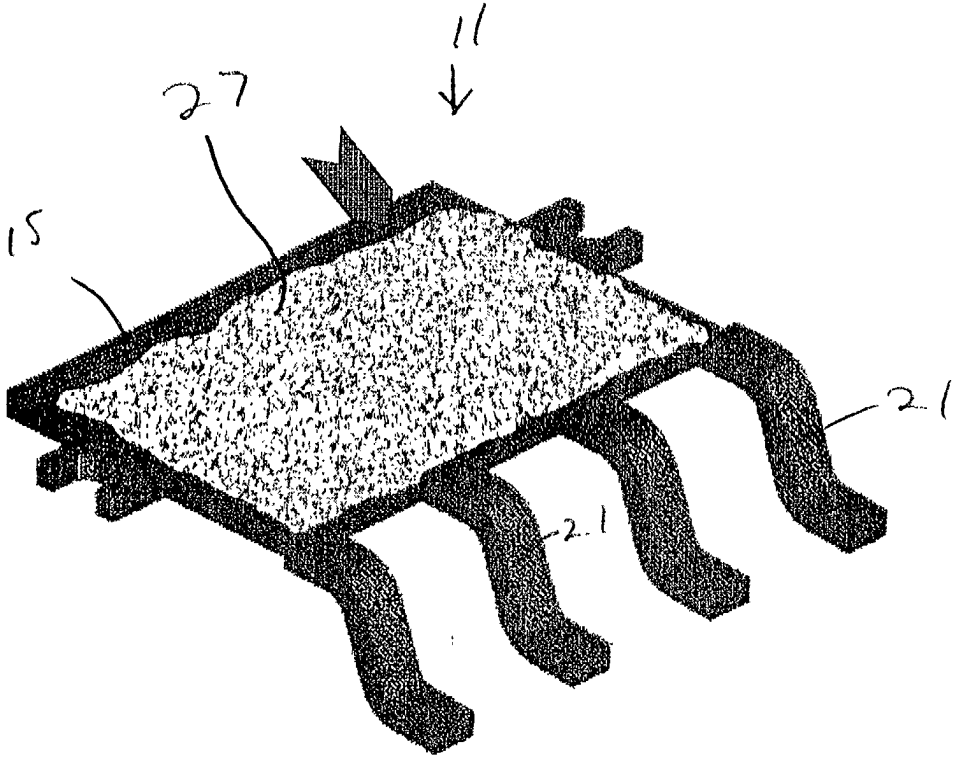

Figure 2B

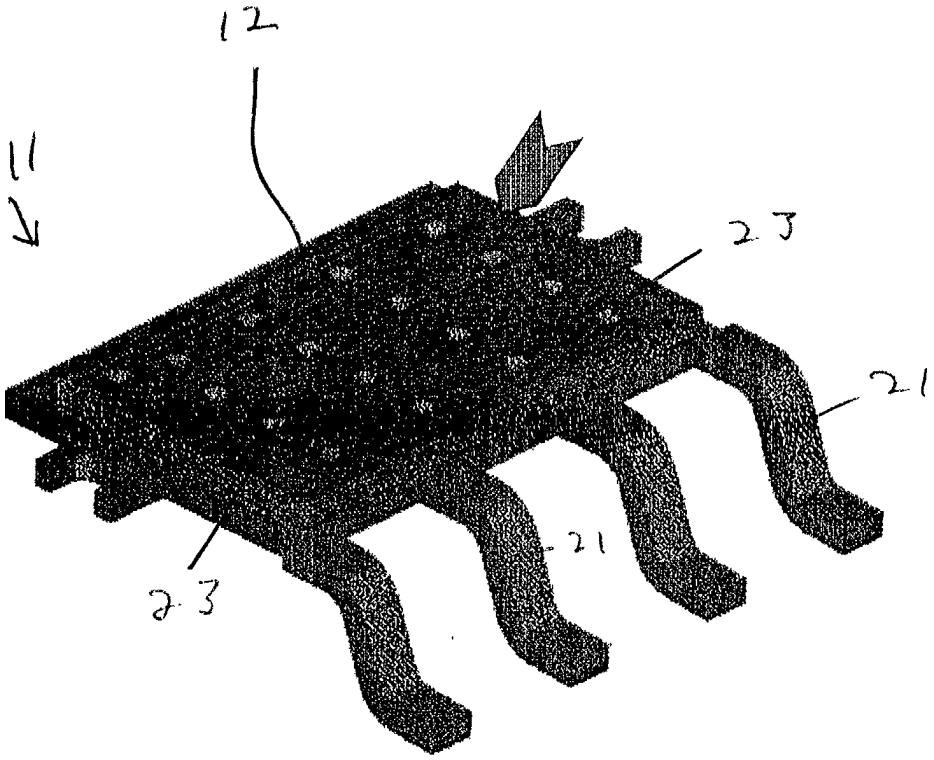

Figure 3A

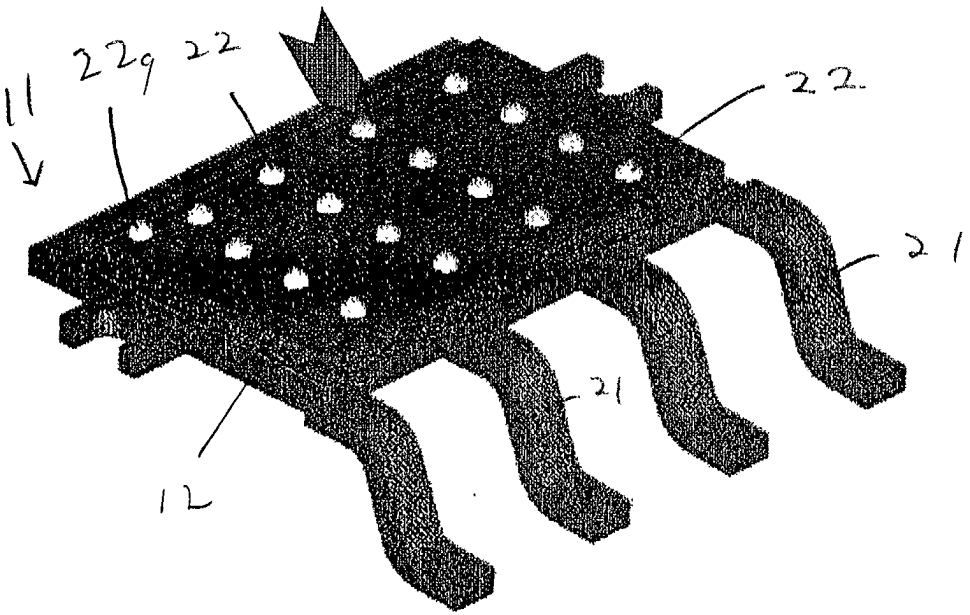

Figure 3B

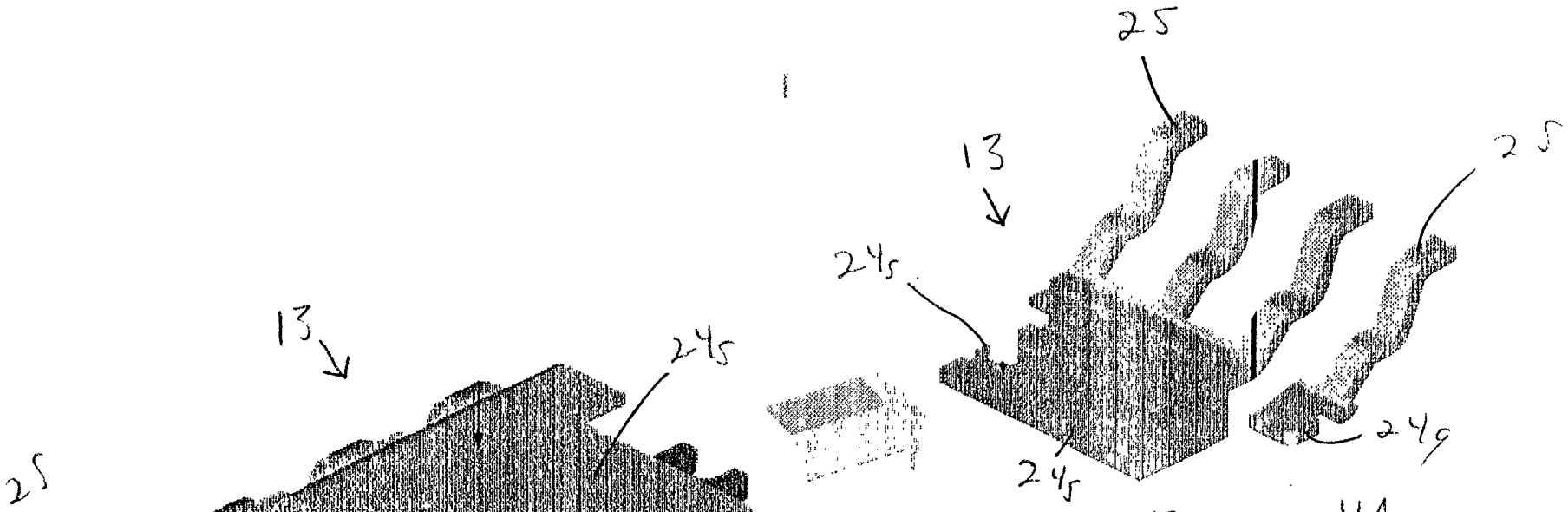

Figure 4A

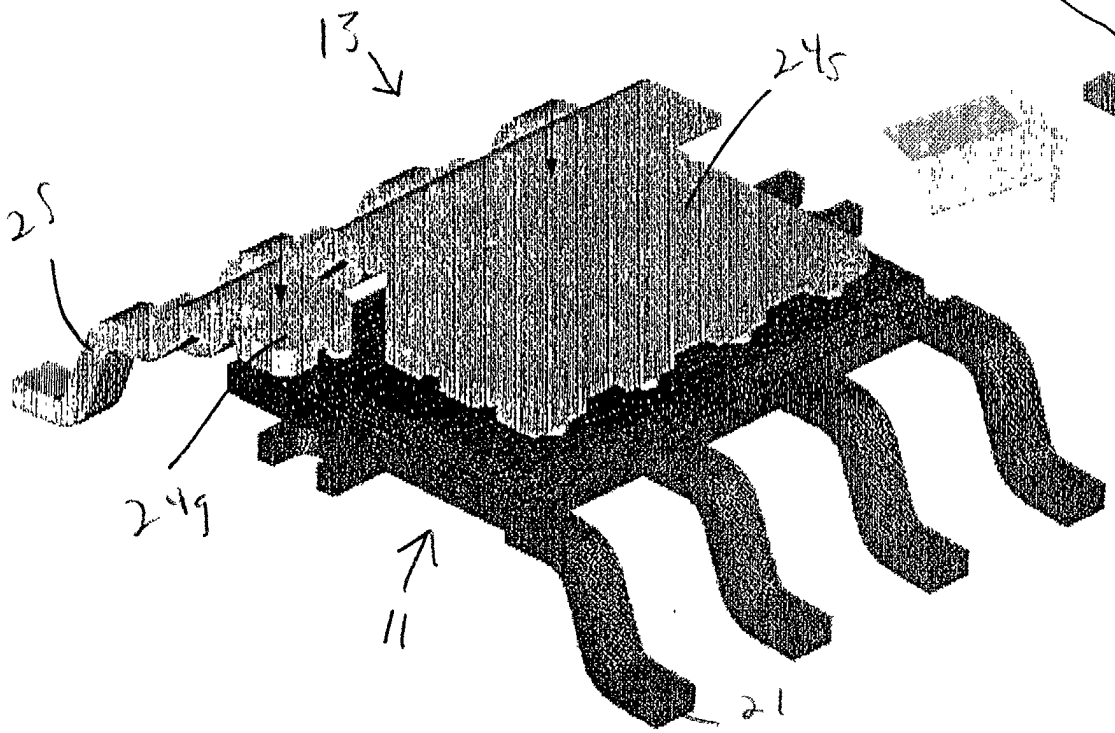

Figure 4B

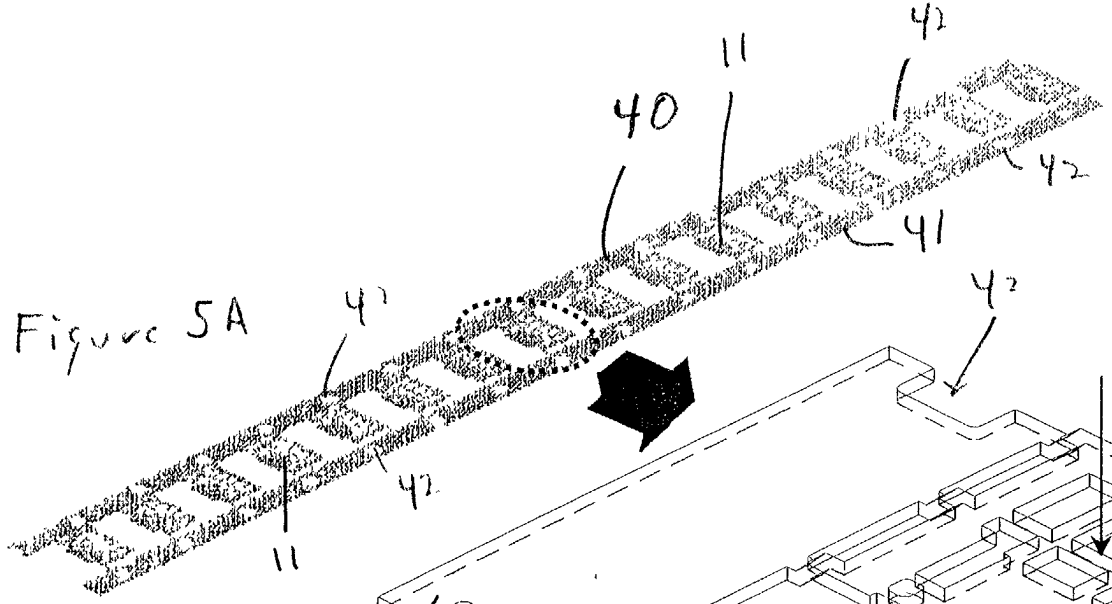

Figure 5A

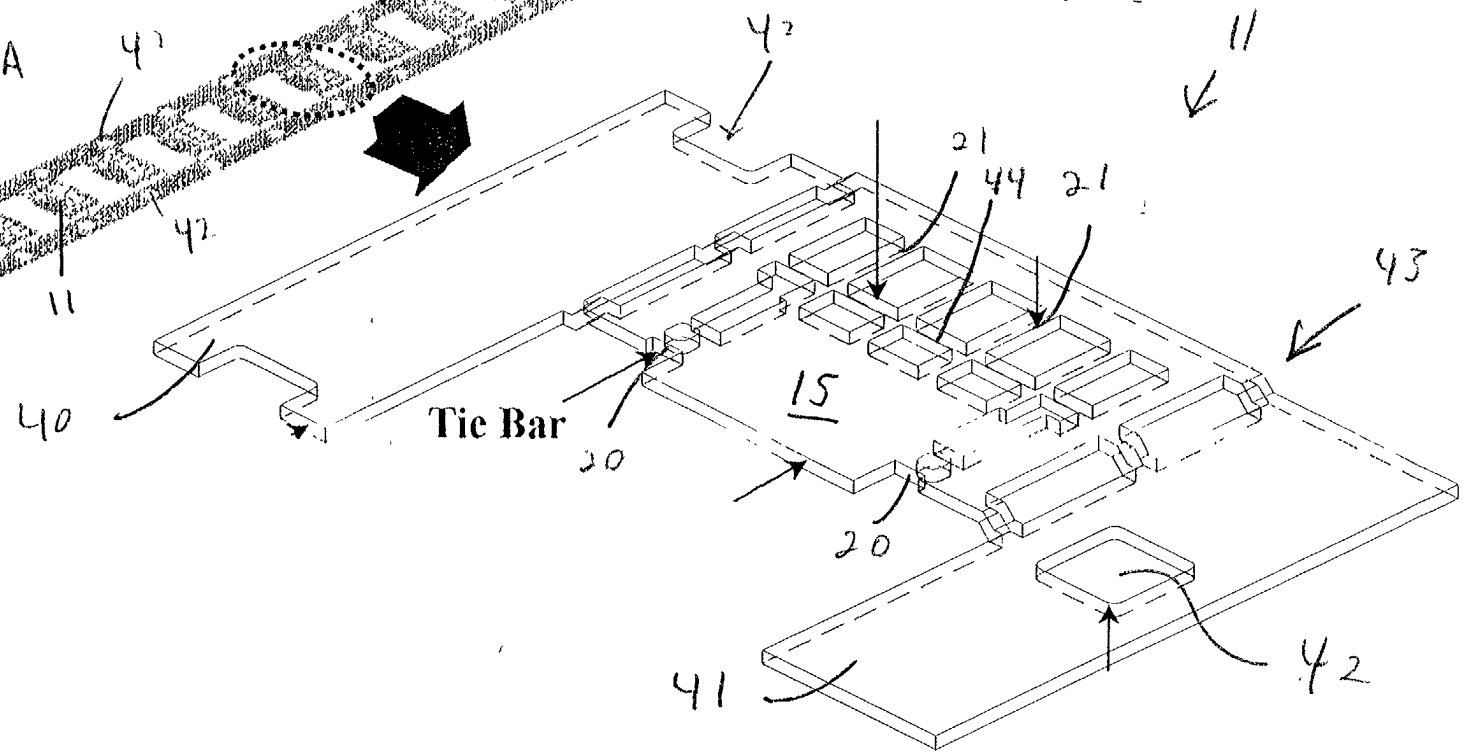

Figure 5B

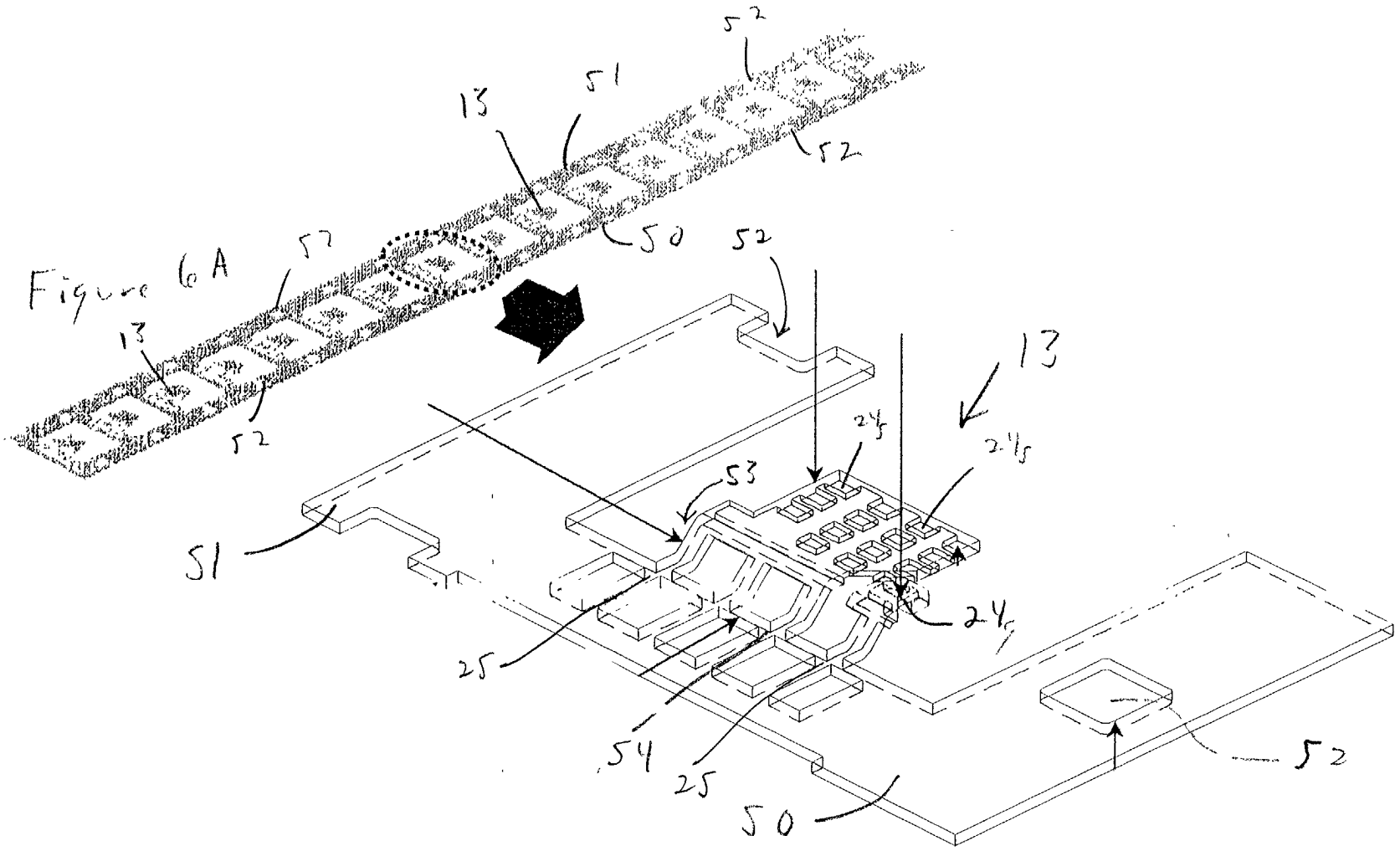

Figure 6A

Figure 6B

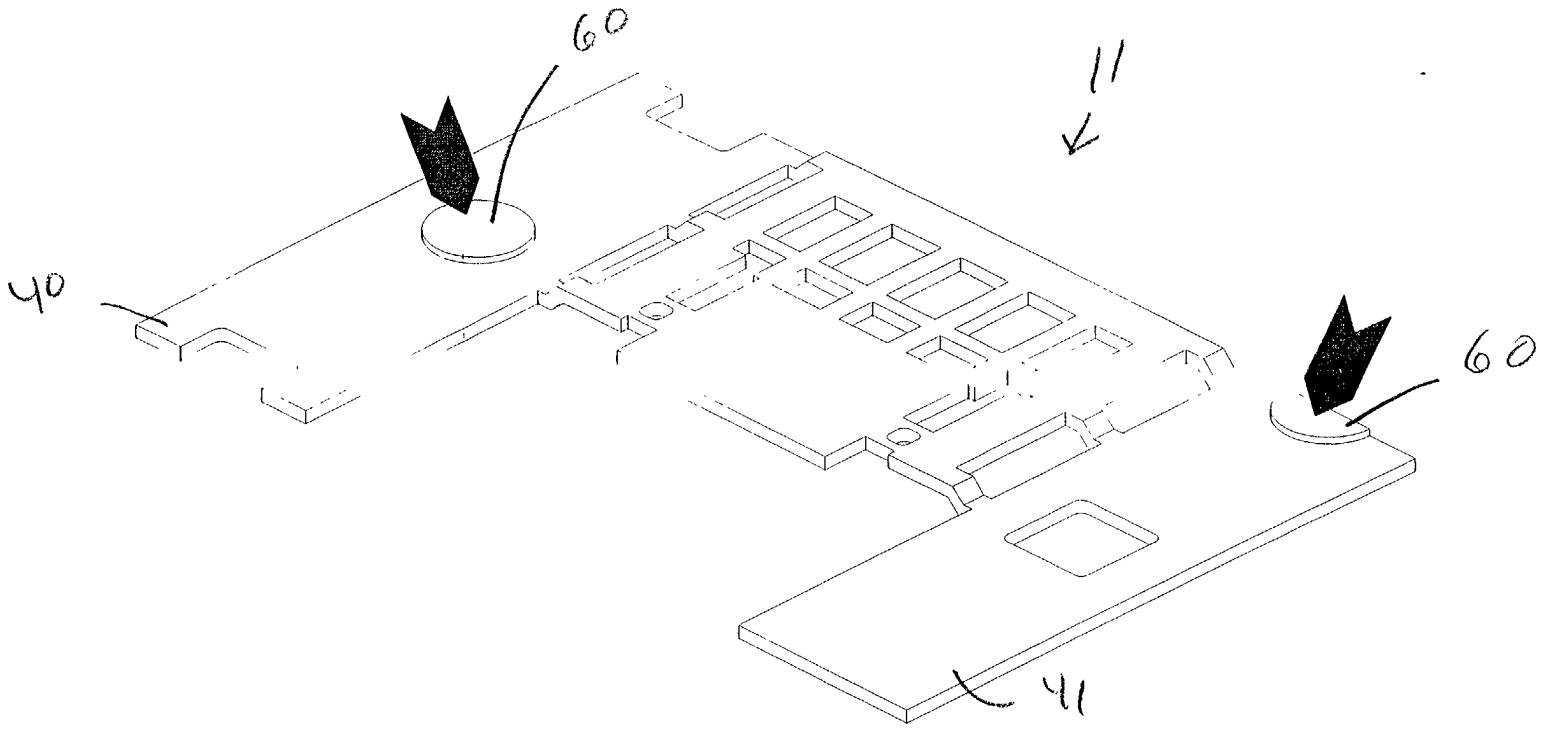

Figure 7

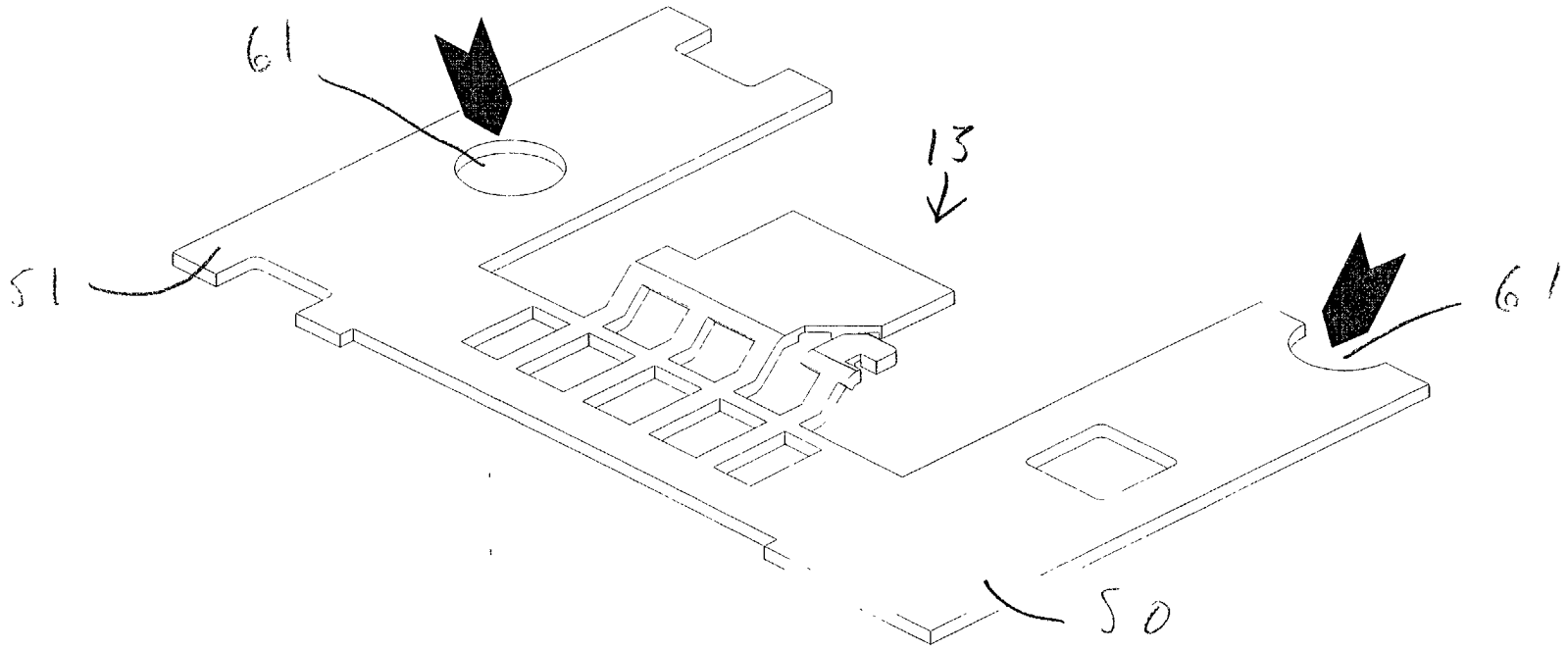

Figure 8

Attorney Docket No.: 18865-35US
Client Reference No.: 17732-9833

DECLARATION

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **IMPROVED METHOD OF MAKING A CHIP DEVICE** the specification of which X is attached hereto or _____ was filed on _____ as Application No. _____ and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

Full Name of Inventor 1:	Last Name: QUINONES	First Name: Maria CLEMENS	Middle Name or Initial: Y.	
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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1 Maria Clemens Y. Quinones Date	Signature of Inventor 2 Gilmore S. Baje Date	Signature of Inventor 3 Maria Christina B. Estacio Date
Signature of Inventor 4 Marvin R. Gestole Date	Signature of Inventor 5 Oliver M. Ledon Date	Signature of Inventor 6 Santos Mepieza Date